A Theoretical Study of the High-Frequency Performance of a Schottky-Barrier Field-Effect Transistor Fabricated on a High-Resistivity Substrate

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The short-circuit admittance parameters for a silicon Schottky-barrier field-effect transistor (SBFET) fabricated on a high-resistivity substrate are calculated from first principles ignoring the effects of minority carriers. The calculations show the maximum frequency of oscillation for a device with a 1-µm gate to be 17.9 GHz, neglecting the parasitic associated with the contact metallizations, and 14.7 GHz when the parasitic are included. In order to describe the dynamic behavior of the device, the static properties must first be obtained. The simultaneous solution of Poisson's equation and the continuity equation, both in two dimensions, gives the static charge and potential distribution in the device. The effects of a field-dependent mobility are included in the continuity equation. Using the results of static two-dimensional solutions, a one-dimensional device model is developed that permits the dynamic device behavior to be described by a one-dimensional linear ordinary differential equation. By solving this equation under appropriate boundary conditions, the device y parameters are found as functions of frequency. Calculated results are shown to be in good agreement with published experimental data.

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